CLAIMS

We claim:

1. A memory unit comprising:

a memory; and

a controller configured to provide unrestricted access for writing information into an unwritten area of said memory, and restricted access for reading said written information.

2. The memory unit according to claim 1, wherein said memory is an NVRAM.

3. The memory unit according to claim 1, wherein said controller is configured to prevent said written information from being overwritten until said memory is completely erased.

4. The memory unit according to claim 1 further comprising a first interface, wherein said controller allows a first device to write said information into said unwritten area through said first interface, but not to read said information once written nor overwrite said written information until said memory is completely erased.

5. The memory unit according to claim 4 further comprising logic, wherein said controller allows said logic exclusive access to read said written information.

6. The memory unit according to claim 5 further comprising a second interface, wherein said controller allows a second device to write said information into said unwritten area through said second interface provided said first device is not writing to said unwritten area at the time, but not to read said written information once written by said first or said second device nor overwrite said written information until said memory is completely erased.

7. The memory unit according to claim 6, wherein said memory is organized into a protected area for storing said information, and an unprotected area for storing other information.

8. The memory unit according to claim 7, wherein said controller allows said first and said second devices to write, read and overwrite said other information in said unprotected area.

9. The memory unit according to claim 8, wherein said protected area is located within said memory according to a pointer as specified during system configuration.

10. The memory unit according to claim 9, wherein said pointer is stored in a manufacturer specified location in said memory.

11. The memory unit according to claim 6, wherein said first interface is a CPU interface and said first device is a CPU.

12. The memory unit according to claim 11, wherein said logic is an authorization unit, and said written information indicates whether software is authorized to be processed by said CPU.

13. The memory unit according to claim 12, wherein said CPU is on the same integrated circuit as the memory unit.

14. The memory unit according to claim 6, wherein said second interface is a JTAG interface and said second device is an external JTAG hardware communicating with said controller using a JTAG protocol.

15. The memory unit according to claim 14, wherein said external JTAG hardware is not on the same integrated circuit as the memory unit.

16. A memory unit comprising:

a memory including a protected area;

a JTAG interface;

logic; and

a controller configured to allow JTAG hardware to write information into said protected area through said JTAG interface, and allow said logic exclusive access to read said written information.

17. The memory unit according to claim 16, wherein said memory is an NVRAM.

18. The memory unit according to claim 16, further comprising a CPU interface coupled to a CPU,

wherein said logic is an authorization unit to authorize software to run on said CPU, and said information indicates whether particular software is authorized to run on said CPU.

19. The memory unit according to claim 18, wherein said memory includes an unprotected area, and said controller allows said CPU to write, read and overwrite other information into said unprotected area through said CPU interface.

20. The memory unit according to claim 18, wherein said controller allows said CPU to write to said memory through said CPU interface provided said JTAG hardware is not writing to said memory at the time.

21. The memory unit according to claim 20, wherein said controller allows said JTAG hardware to write to said memory through said JTAG interface provided said CPU has not issued a request to write to said memory at the time.

22. The memory unit according to claim 20, wherein said CPU interface and said JTAG interface are clocked by different clock signals so that said controller includes at least one synchronization buffer to synchronize communications received from said CPU interface and said JTAG interface.

23. The memory unit according to claim 22, wherein said controller waits for a synchronization delay period related to said at least one synchronization buffer

before granting said JTAG interface access to write to said memory, if said CPU is not writing to said memory at a start of said synchronization delay period and does not initiate a write to said memory before an end of said synchronization delay period.

24. The memory unit according to claim 22, wherein said at least one synchronization buffer includes:

a first buffer for synchronizing signals between said JTAG interface and said controller; and

a second buffer for synchronizing signals between said CPU interface and said controller.

25. A memory unit comprising:

a memory;

a JTAG interface clocked by a JTAG clock signal received from an external JTAG hardware; and

a controller configured to allow said external JTAG hardware to write information into said memory through said JTAG interface, wherein said controller is clocked either by a system clock signal or by said JTAG clock signal if said system clock signal is not available.

26. The memory unit according to claim 25, wherein said memory is an NVRAM.

27. The memory unit according to claim 25, further comprising a CPU interface coupled to a CPU, wherein said CPU is clocked by said system clock signal, and said controller is configured to allow said CPU to write information into said memory through said CPU

interface provided said external JTAG hardware is not writing to said memory at the time.

28. The memory unit according to claim 27, wherein said system clock signal is generated in an integrated circuit including said JTAG interface, said CPU interface, said CPU, and said controller; and said JTAG clock signal is provided to said integrated circuit by said external JTAG hardware.

29. The memory unit according to claim 28, wherein said controller includes a first synchronization buffer for synchronizing signals between said JTAG interface and said controller when said controller is clocked by said system clock signal.

30. The memory unit according to claim 29, wherein said CPU interface is clocked by an IP-bus clock signal, and said controller includes a second synchronization buffer for synchronizing signals between said CPU interface and said controller.

31. The memory unit according to claim 30, wherein said controller waits for a synchronization delay period related to said first and said second synchronization buffers before granting said JTAG interface access to write to said memory, if said CPU is performing a write to said memory at a start of said synchronization delay period and said CPU does not initiate another write to said memory before an end of said synchronization delay period.

32. A memory unit comprising:

a non-volatile memory storing a first boot configuration vector; and

a reset circuit coupled to said non-volatile memory and a plurality of external boot configuration vector pins, wherein said reset circuit generates one or more initialization signals upon activation using said first boot configuration vector if a status of a designated one of said plurality of external boot configuration vector pins is a first state or using a second boot configuration vector provided on others of said plurality of external boot configuration pins if the status of said designated one of said external boot configuration vector pins is a second state.

33. The memory unit according to claim 32, wherein said non-volatile memory is an NVRAM.

34. The memory unit according to claim 32, further including a CPU interface coupled to a CPU, a JTAG interface coupled to at least one external pin, and a controller coupled to said non-volatile memory, said CPU interface, and said JTAG interface, wherein said CPU is clocked by a system clock signal generated in an integrated circuit device including said JTAG interface, said CPU interface, said CPU and said controller; and said JTAG interface is clocked by a JTAG clock signal provided from an external JTAG hardware coupled to said JTAG interface through said at least one external pin.

35. The memory unit according to claim 34, wherein said controller allows either one of said CPU and

said external JTAG hardware to write said first boot configuration vector in said NVRAM, provided the other one of said CPU and said external JTAG hardware is not writing said boot configuration vector in said NVRAM at the time.

36. The memory unit according to claim 34, wherein said controller is clocked by said system clock signal provided said system clock signal is available, or clocked by said JTAG clock signal if said system clock signal is not available.

37. The memory unit according to claim 36, wherein said controller allows said external JTAG hardware to write said first boot configuration vector in said NVRAM through said JTAG interface before said CPU boots up.